

CODE	TITLE	APPLICATION / DESCRIPTION
VTVL01	An Efficient Light-weight Configurable Approximate Adder Design	Description: A Light-weight Configurable Approximate Adder (LCAA) based on the traditional accurate mirror adder with only 2 extra transistors. This more efficient design can dynamically switch between the accurate and approximate mode at runtime with better tradeoff of the power and accuracy
VTVL02	Design of a 32-bit Accuracy-Controllable Approximate Multiplier for FPGAs	Description: Approximate multiplier has a special input to dynamically control the accuracy, in addition to two operands. The special input allows the multiplier to perform fast multiplication when high accuracy is not required and slow multiplication when high accuracy is required
VTVL03	A modified high speed and less area BCD adder architecture using Mirror adder	Description: Mirror adder is an adder circuit which is implemented without using XOR gates. BCD adder architecture is modified by replacing the 4-bit RCA with 4-bit mirror adder.
VTVL04	Design and Analysis of High-Performance Carry Skip Adder using Various Full Adders	Description: A correlative analysis of several adders like Carry Save Adder (CSaA), Carry Select Adder (CSeA), Carry Skip Adder (CSA), Ripple Carry Adder (RCA), Carry Look ahead Adder (CLA) designed and analyzed using Verilog HDL code.
VTVL05	Design of 16-Bit and 32-Bit Approximate Full Adder Using Majority Logic	Description: A 16-bit and 32-bit Approximate Full Adder based on Majority Logic. Use of approximate computing increases the storage capacity. The Majority Logic has become a basic gate for most of advanced circuits
VTVL06	Power Efficient and High-performance 4-bit Dadda Multiplier using Multiplexer based BEC-1 converter	Description: The dadda multiplier has become the most popular tree multiplier due to its high computational speed and low hardware configuration. Most of the delay of the dadda multiplier depends on the partial and final sum of the product. Energy-saving full adders and half adders are used to reduce the total power requirement of the dadda multiplier.
VTVL07	Design and Implementation of Low Power and High- Speed Full Adder	Description: Combination of different logic styles are used to implement adder circuits. Here, XOR-XNOR and full adder (FA) implemented using PTL, CPL cross coupled and PTL cross coupled logic styles
VTVL08	Development of Floating-Point MAC Engine for 2-D Convolution of Image	Description: A single-precision Floating Point MAC engine to accelerate the sliding window algorithm for the 2-D convolution of image. The engine uses a modified algorithm for virtual zero-padding that saves memory space, and it also provides configurable parameters to specify filter and image size
VTVL09	A High-Speed Floating-Point Multiply-Accumulator Based on FPGAs	Description: A novel high-speed floating-point multiply-accumulator (FPMAC) with a signed soft multiplier and a single-cycle floating-point accumulator (FAAC).

CODE	TITLE	APPLICATION / DESCRIPTION	IEEE 2021 - FPGA & DIGITAL DESIGN
VTVL10	Design and Analysis of Approximate 4–2 Compressors for High-Accuracy Multipliers	Description: A five high-accuracy approximate 4–2 compressors with better delay, area, power, and better performance–accuracy tradeoff. Pro1–Pro4 rely on the critical path optimization, while Pro5 derives from the modified sorting technique	
VTVL11	Inexact Signed Wallace Tree Multiplier Design Using Reversible Logic	Description: An inexact Baugh-Wooley Wallace tree multiplier with novel architecture for inexact 4:2 compressor optimised for realisation using reversible logic. The inexact 4:2 compressor has ± 1 Error Distance (ED) and 12.5% Error Rate (ER).	
VTVL12	Low Area and High Throughput Architectures of FIR Filter for Data Streaming DSP Applications	Description: This article attempts to develop hardware architectures for FIR Filter and apply the design optimization techniques present in literature. In this article, High Level Synthesis concepts were adapted to develop hardware architecture for FIR filter and optimization techniques have been applied to optimize design attributes like area, throughput and power	
VTVL13	Design and Analysis of Approximate Compressors for Balanced Error Accumulation in MAC Operator	Description: A novel approximate computing scheme suitable for realizing the energy-efficient multiply-accumulate (MAC) processing. We utilize different approximate multipliers in an interleaved way to compensate errors in the opposite direction during accumulate operations	
VTVL14	Design of an Accurate, Cost-effective Radix-4 Booth Multiplier	Description: An optimized algorithm and multiplier for accurate radix-4 booth multiplication. The algorithm reduces the number of bits that participate in the addition process during multiplication	
VTVL15	Implementation of 256 Bit Key AES Algorithm with Key Schedule and Sub Bytes Block Optimization	Description: The proposed 256-bit AES algorithm is highly optimized in Key schedule and Sub bytes blocks, for Area and Power. The optimization has been done by reusing the S-box block	